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(71)Applicant : TOSHIBA CORP

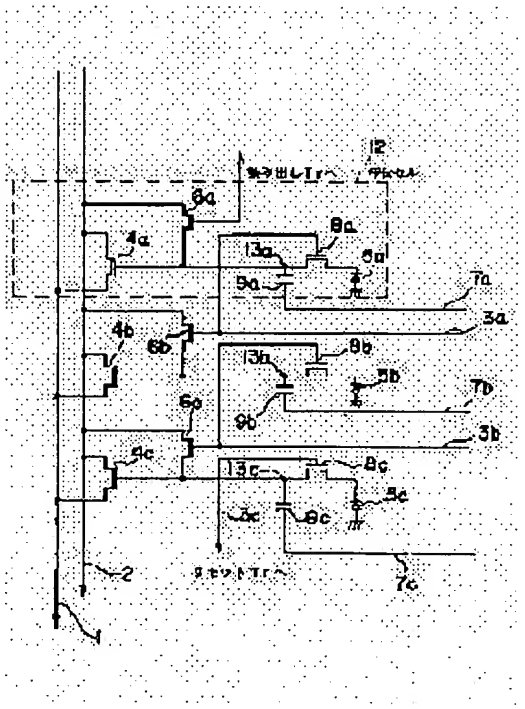
(72)Inventor : IHARA HISANORI
MIYAGAWA RYOHEI
TANAKA NAGATAKA
YAMAGUCHI TETSUYA
IIDA YOSHINORI
NOZAKI HIDETOSHI
MABUCHI KEIJI
YAMASHITA HIROSHI
OBA HIDEFUMI
SASAKI MICHIO

(54) SOLID-STATE IMAGING DEVICE AND DRIVING METHOD THEREOF

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a solid-state imaging device in which elements can be made small in size.

SOLUTION: In the solid-state imaging device having a plurality of unit cells arranged in row and column directions, there is provided a wiring line 3a for transmission of a signal for turning on at least one transfer gate 8a in the unit cell and for transmission of a signal for turning on a reset gate 6b in the unit cell adjacent in the column direction to the unit cell.



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CLAIMS

[Claim(s)]
[Claim 1] In the solid state camera which has arranged two or more unit cells in the matrix direction said unit cell At least one photo-electric-conversion means to change light into a charge, and a charge maintenance means to hold the charge outputted from said at least one photo-electric-conversion means, The transfer gate which transmits the charge which was connected, respectively and was outputted from said photo-electric-conversion means between said at least one photo-electric-conversion means and said charge maintenance means in ON for said charge maintenance means, It has the reset gate which resets the charge held at said charge maintenance means in ON. The solid state camera characterized by providing wiring which transmits the signal for turning ON the reset gate of said unit cell which transmits the signal for turning ON at least one transfer gate of a part of unit cells, and adjoins in the direction of a train to said a part of unit cells.
[Claim 2] The threshold of the reset gate of the unit cell which adjoins in said direction of a train is a solid state camera according to claim 1 characterized by being a value smaller than the threshold of the transfer gate of a part of said unit cells.
[Claim 3] At least one photo-electric-conversion means to change light into a charge, and a charge maintenance means to hold the charge outputted from said at least one photo-electric-conversion means, The transfer gate which transmits the charge which was connected, respectively and was outputted from said photo-electric-conversion means between said at least one photo-electric-conversion means and said charge maintenance means in ON for said charge maintenance means, The reset gate which resets the charge held at said charge maintenance means in ON, The unit cell equipped with a voltage-output means to output the electrical potential difference corresponding to the charge held at said charge maintenance means is arranged in the direction of a multi-line train. The signal for turning ON at least one transfer gate of a part of unit cells is transmitted. And it sets to the drive approach of a solid state camera of having provided wiring which transmits the signal for turning ON the reset gate of said unit cell which adjoins in the direction of a train to said a part of unit cells. While resetting the charge held at said charge maintenance means of the unit cell which turns ON the reset gate of said unit cell which impresses an electrical potential difference to said wiring, and adjoins in the direction of a train, and adjoins in said direction of a train The charge which turned ON at least one transfer gate of a part of said unit cells, and was outputted from said photo-electric-conversion means of a part of said unit cells is transmitted to said charge maintenance means. The drive approach of the solid state camera characterized by outputting the electrical potential difference corresponding to the charge held by said voltage-output means at the charge maintenance means of a part of said unit cells.
[Claim 4] In the solid state camera equipped with two or more unit cells said unit cell A charge maintenance means to hold the charge outputted from a photo-electric-conversion means to change light into a charge, The resetting means which resets the charge held at said charge maintenance means in ON, It has an address means to output the electrical potential difference corresponding to the charge held at said charge maintenance means in ON. The solid state camera characterized by providing further wiring which transmits the signal for transmitting the signal for turning ON said resetting means of a part of unit cells, and turning ON said address means of a part of said unit cells.
[Claim 5] A charge maintenance means to hold the charge outputted from a photo-electric-conversion means to change light into a charge, The resetting means which resets the charge held at said charge maintenance means in ON, It has two or more unit cells equipped with an address means to output the electrical potential difference corresponding to the charge held at said charge maintenance means in ON. In the drive approach of a solid state camera of having provided further wiring which transmits the signal for transmitting the signal for turning ON said resetting means of a part of unit cells, and turning ON said address means of a part of said unit cells The charge which impressed the electrical potential difference to said wiring, turned ON said resetting means of a part of said unit cells, and was held at said charge maintenance means of a part of said unit cells is reset. The drive approach of the solid state camera

characterized by outputting the electrical potential difference corresponding to the charge which impressed the electrical potential difference to said wiring, turned ON the address means of a part of said unit cells, and was held at said charge maintenance means.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to a solid state camera and its drive approach.
[0002]
[Description of the Prior Art] The solid state camera which gave the magnification function to the interior of a pixel in modulating the potential of the signal-charge are recording section by the signal charge generated by photo electric conversion, and modulating the magnification transistor inside a pixel with the potential is called a magnification mold solid state camera, and is expected as a solid state camera suitable for contraction of the pixel size by the increment in the number of pixels, or contraction of an image size.
[0003] The basic configuration of the pixel in a magnification mold solid state camera The read-out transistor for reading a charge from the photodiode for performing photo electric conversion, and this photodiode, And the reset transistor for [which reads and discharges a line and a signal charge] having connected with the gate of this read-out transistor, And it is wiring (address line) which connects the transistor for the magnification transistor for the reset line connected to the gate of this reset transistor, and signal magnification, and the Rhine selection or capacity, and a photodiode and the gate of a magnification transistor.
[0004] Furthermore, wiring (drain wire) for discharging wiring (signal line) for reading the signal amplified with the magnification transistor and a signal charge is wired, respectively. Usually, wiring for a read-out line, a reset line, and the Rhine selection (address line), the signal line, and the drain wire are wired independently, respectively.
[0005]
[Problem(s) to be Solved by the Invention] As mentioned above, in the conventional magnification mold solid state camera, at least five need to be wired, such as the address line for the reset line wired at the gate of the reset transistor for [which reads and discharges a line and a signal charge] having wired at the gate of a signal line, a drain wire, and a read-out transistor, and the Rhine selection, and these were wiring independently.
[0006] For this reason, when detailed-ization of a component was performed, there was a problem that spacing of wiring will become short and will become a short cause. Moreover, in order to have to perform these wiring through an insulator layer etc., there was a problem of a level difference arising within a component and causing an open circuit of wiring.
[0007] Furthermore, in order to wire many, the configuration was complicated, and there was a problem of having faced performing detailed-ization of a component and becoming a failure. Moreover, the solid state camera which has the wiring configuration of the unit cell for which it was suitable in order to perform detailed-ization of a component is known.
[0008] Drawing 10 is drawing showing the configuration of the unit cell of such a solid state camera, and drawing 11 is drawing showing the layout of such a unit cell. In this drawing, although only three unit cells are shown, the unit cell shall be arranged in the shape of two-dimensional. Moreover, as shown in this drawing, the unit cell 121 is equipped with photodiode 115a which changes light into a charge, address transistor 117a which chooses Rhine which reads a signal charge, magnification transistor 114a which amplifies the detecting signal of a photodiode and is outputted to a signal line 1, and reset transistor 116a which resets the charge accumulated in the detecting element.
[0009] Here, although a unit cell 121 is explained, the configuration with the same said of other unit cells shall be adopted. The gate of address transistor 117b of a unit cell and the gate of reset transistor 116a which adjoin in the direction of a train to a unit cell 112 are connected to the address / reset line 113a. The address / reset line 113a transmits the signal for resetting the charge accumulated in the signal and detecting element for choosing the readout line from a perpendicular shift register.

[0010] Moreover, the drain of reset transistor 116a is connected to the detecting element, and the source is connected to the drain wire 112 for discharging the charge accumulated in the detecting element. The gate of magnification transistor 114a is connected to a detecting element, a drain is connected to a drain wire 112, and the source is connected to the signal line 111.
[0011] In the solid state camera which has the unit cell of a configuration as shown in drawing 10 , the problem of realizing detailed-ization of the component which is an above-mentioned trouble is solvable. However, in the solid state camera which has the unit cell of such a configuration, the address / reset line performs ON independently for the reset transistor of ON of the address transistor of the unit cell which adjoins the direction lower part of a train, and the unit cell of the direction upper part of a train, respectively.
[0012] In this case, to a drain wire 112, the drain current which flows by turning on the reset current and address transistor which flow by turning on a reset transistor flows.
[0013] Therefore, the potential of a drain wire 112 had to adjust the potential of the drain of a reset transistor, and the source potential of a magnification transistor, and had the problem that an excessive burden will be placed on a drain wire 112.
[0014] This invention is made in view of the above-mentioned actual condition, and aims at offering the solid state camera which can realize detailed-ization of a component easily, and its drive approach. Moreover, this invention aims at offering the solid state camera which enables implementation of detailed-izing of a component, and does not apply a burden to a drain wire, and its drive approach.
[0015]
[Means for Solving the Problem] First in order to attain the above-mentioned purpose therefore, the 1st invention In the solid state camera which has arranged two or more unit cells in the matrix direction said unit cell At least one photo-electric-conversion means to change light into a charge, and a charge maintenance means to hold the charge outputted from said at least one photo-electric-conversion means, The transfer gate which transmits the charge which was connected, respectively and was outputted from said photo-electric-conversion means between said at least one photo-electric-conversion means and said charge maintenance means in ON for said charge maintenance means, It has the reset gate which resets the charge held at said charge maintenance means in ON. It is characterized by providing wiring which transmits the signal for turning ON the reset gate of said unit cell which transmits the signal for turning ON at least one transfer gate of a part of unit cells, and adjoins in the direction of a train to said a part of unit cells.
[0016] Moreover, it is characterized by the threshold of the reset gate of a unit cell where the 2nd invention adjoins in said direction of a train in the 1st invention being a value smaller than the threshold of the transfer gate of a part of said unit cells.
[0017] Furthermore, at least one photo-electric-conversion means by which the 3rd invention changes light into a charge, A charge maintenance means to hold the charge outputted from said at least one photo-electric-conversion means, The transfer gate which transmits the charge which was connected, respectively and was outputted from said photo-electric-conversion means between said at least one photo-electric-conversion means and said charge maintenance means in ON for said charge maintenance means, The reset gate which resets the charge held at said charge maintenance means in ON, The unit cell equipped with a voltage-output means to output the electrical potential difference corresponding to the charge held at said charge maintenance means is arranged in the direction of a multi-line train. The signal for turning ON at least one transfer gate of a part of unit cells is transmitted. And it sets to the drive approach of a solid state camera of having provided wiring which transmits the signal for turning ON the reset gate of said unit cell which adjoins in the direction of a train to said a part of unit cells. While resetting the charge held at said charge maintenance means of the unit cell which turns ON the reset gate of said unit cell which impresses an electrical potential difference to said wiring, and adjoins in the direction of a train, and adjoins in said direction of a train The charge which turned ON at least one transfer gate of a part of said unit cells, and was outputted from said photo-electric-conversion means of a part of said unit cells is transmitted to said charge maintenance means. It is characterized by outputting the electrical potential difference corresponding to the charge held by said voltage-output means at the charge maintenance means of a part of said unit cells.
[0018] In the solid state camera with which the 4th invention was equipped with two or more unit cells furthermore, said unit cell A charge maintenance means to hold the charge outputted from a photo-electric-conversion means to change light into a charge, The resetting means which resets the charge held at said charge maintenance means in ON, It has an address means to output the electrical potential difference corresponding to the charge held at said charge maintenance means in ON. It is characterized by providing further wiring which transmits the signal for transmitting the signal for turning ON said resetting means of a part of unit cells, and turning ON said address means of a part of said unit cells.

[0019] Furthermore, a charge maintenance means to hold the charge outputted from a photo-electric-conversion means by which the 5th invention changes light into a charge, The resetting means which resets the charge held at said charge maintenance means in ON, It has two or more unit cells equipped with an address means to output the electrical potential difference corresponding to the charge held at said charge maintenance means in ON. In the drive approach of a solid state camera of having provided further wiring which transmits the signal for transmitting the signal for turning ON said resetting means of a part of unit cells, and turning ON said address means of a part of said unit cells The charge which impressed the electrical potential difference to said wiring, turned ON said resetting means of a part of said unit cells, and was held at said charge maintenance means of a part of said unit cells is reset. It is characterized by outputting the electrical potential difference corresponding to the charge which impressed the electrical potential difference to said wiring, turned ON the address means of a part of said unit cells, and was held at said charge maintenance means.

[0020] Next, an operation of each invention is explained. First, the 1st invention transmits the signal for turning ON at least one transfer gate of a part of unit cells. And since wiring which transmits the signal for turning ON the reset gate of said unit cell which adjoins in the direction of a train to said a part of unit cells is provided As compared with the case where wiring which transmits the signal for turning ON wiring and the reset gate which transmit the signal for turning ON the transfer gate is prepared separately, detailed-ization of a unit cell is easily realizable.

[0021] In the solid state camera of the 1st invention, since the 2nd invention makes the threshold of the reset gate of the unit cell which adjoins in the direction of a train the value smaller than the threshold of the transfer gate of a part of said unit cells, it can control a reset gate independently.

[0022] The 3rd invention transmits the signal for turning ON at least one transfer gate of a part of unit cells. And an electrical potential difference is impressed to wiring which transmits the signal for turning ON the reset gate of said unit cell which adjoins in the direction of a train to said a part of unit cells. While resetting the charge held at the charge maintenance means of the unit cell which turns ON the reset gate of said unit cell which adjoins in the direction of a train, and adjoins in said direction of a train The charge which turned ON at least one transfer gate of a part of said unit cells, and was outputted from the photo-electric-conversion means of a part of said unit cells is transmitted to a charge maintenance means. Since the electrical potential difference corresponding to the charge held by the voltage-output means at the charge maintenance means of a part of said unit cells is outputted, the solid state camera possessing shared wiring which connects the transfer gate and a reset gate can be driven.

[0023] The 4th invention can offer a solid state camera with few image defects by providing wiring which transmits the signal for transmitting the signal for turning ON the resetting means of a part of unit cells, and turning ON the address means of a part of said unit cells.

[0024] The 5th invention resets the charge which impressed the electrical potential difference to wiring which transmits the signal for transmitting the signal for turning ON the resetting means of a part of unit cells, and turning ON the address means of a part of said unit cells, turned ON the resetting means of a part of said unit cells, and was held at the charge maintenance means of a part of said unit cells.

[0025] Next, since the electrical potential difference corresponding to the charge which impressed the electrical potential difference to wiring, turned ON the address means of a part of said unit cells, and was held at the charge maintenance means is outputted, the solid state camera possessing wiring which shares an address means and a resetting means within 1 unit cell can be driven.

[0026]

[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained with reference to a drawing.

<Gestalt of the 1st operation> drawing 1 is drawing showing the configuration of the unit cell of the magnification mold solid state camera concerning the gestalt of operation of the 1st of this invention. in addition, drawing 1 -- if it is, the configuration of 3 unit cells is shown and it is the magnification mold solid state camera of a 1-pixel 1 unit-cell configuration.

[0027] In this drawing, although only three unit cells are shown, the unit cell of the magnification mold solid state camera of the gestalt of this operation shall be arranged in the shape of two-dimensional. It has magnification transistor 4a which amplifies the detecting signal of read-out transistor 8a for a unit cell 12 to read the charge accumulated in photodiode 5a which changes light into a charge, and photodiode 5a to detecting-element 13a, address capacity 9a which chooses Rhine which reads a signal charge, and a photodiode as shown in this drawing, and is outputted to a signal line 1, and reset transistor 6a which resets the charge accumulated in detecting-element 13a.

[0028] Here, although the unit cell 12 was explained, the configuration with the same said of other unit cells shall be adopted. It connects with read-out / reset line 3a with the common gate of reset transistor 6b of the unit cell which

adjoins in the gate and the direction of a train of readout transistor 8a. Read-out / reset line 3a transmits the signal for turning ON reset transistor 6b of the unit cell which adjoins in readout transistor 8a from a perpendicular shift register, and the direction of a train.
[0029] Moreover, the end of address capacity 9a is connected to address-line 7a. Address-line 7a transmits the signal for choosing the readout line from a perpendicular shift register.
[0030] The gate of reset transistor 6a is connected to the readout transistor of the unit cell which adjoins the direction upper part of a train, and common wiring. This wiring transmits the signal for resetting the charge accumulated in detecting-element 13a from a perpendicular shift register.
[0031] Moreover, the drain of reset transistor 6a is connected to detecting-element 13a, and the source is connected to the drain wire 2 for discharging the charge accumulated in detecting-element 13a.
[0032] The gate of magnification transistor 4a is connected to detecting-element 13a, a drain is connected to a drain wire 2, and the source is connected to the signal line 1. The noise canceller for removing the noise of the signal outputted to the signal line 1 is formed in this signal line 1.
[0033] And the signal with which the noise outputted from the noise canceller was removed is outputted to a level signal line one by one through the level selection transistor driven by the selection pulse supplied from a level shift register.
[0034] Next, the formation approach of the magnification mold solid state camera of such a configuration is explained with reference to the planar structure Fig. of drawing 2 . This magnification mold solid state camera is p+10 (component isolation region) and n+ to the surface layer of a p-type silicon semi-conductor substrate. Layers (photodiode) 5a-5c are formed, and a signal charge is generated in this photodiode section 5.
[0035] And n layers are formed in the field which forms the readout transistors 8a-8c and the reset transistors 6a-6c. Then, a front face is covered with an oxide film and an electrode wiring material (for example, polish recon) is deposited further.
[0036] And in order to form the gate and the reset line of the read-out transistors 8a-8c, the read-out / reset lines 3a-3c, and the reset transistors 6a-6c, an electrode wiring material is processed and read to a desired configuration, and a line and wiring of a reset transistor are formed. Since a readout line and a reset line are made to serve a double purpose at this time, patterning can be carried out at once and read-out / reset lines 3a-3c can be formed.
[0037] Then, after forming the component part of a magnification mold solid state camera as mentioned above, wiring (drain wire 2) for discharging wiring (signal line 1) for reading the signal current and a signal charge is wired.
[0038] In drawing 2 , only the contact section for obtaining a signal line 1, a drain wire 2, and an electric flow is illustrated. A signal line 1 and a drain wire 2 wire in the vertical direction, and obtain an electric flow in the contact section.
[0039] Moreover, in drawing 2 , as a wiring material, although polish recon is used, a metal alloy including at least one or more kinds of metals, such as an amorphous silicon which mixed the impurity, AI (aluminum), a tungsten (W), MORIBURITEN (Mo), and titanium (Ti), or said metal, and the compound which makes a SHIRIZAIDO compound the start can also be used.
[0040] Next, with reference to the timing chart of drawing 3 , actuation of the magnification mold solid state camera of the gestalt of this operation is explained. First, the transfer pulse 21 is added in horizontal blanking interval H-BLK1 at read-out / reset line 3a, the signal charge of photodiode 5a is read to detecting-element 13a, and it accumulates in address capacity 9a.
[0041] At this time, reset transistor 6b of the unit cell which adjoins the direction lower part of a train at coincidence is turned on, reset of the charge accumulated in detecting-element 13b is performed, and the charge accumulated in detecting-element 13b is discharged by the drain wire 2.
[0042] Next, the address pulse 22 is impressed to address capacity 9a through address-line 7a. By impressing the address pulse 22 to address capacity 9a, the potential of the channel of magnification transistor 4a rises as compared with other Rhine, and a source follower circuit is constituted by a load transistor and magnification transistor 4a.
[0043] Therefore, an electrical potential difference with the signal charge of photodiode 5a almost equal to the signal level by which impedance conversion was carried out is outputted to a signal line 1. The signal outputted to this signal line 1 is outputted to a level signal line by being chosen with a level shift register through a noise rejection circuit.
[0044] Thus, after sampling the output voltage of the photodiode of the 1st line, within the next horizontal blanking interval, the transfer pulse 23 is similarly impressed to read-out / reset line 3b of the 2nd Rhine, the signal charge of photodiode 5b of the 2nd Rhine is read to detecting-element 13b, and it accumulates in address capacity 9b.
[0045] At this time, reset transistor 6c of the unit cell which adjoins the direction lower part of a train at coincidence is turned on, reset of the charge accumulated in detecting-element 13c is performed, and the charge accumulated in

detecting-element 13c is discharged by the drain wire 2.
[0046] Next, the address pulse 24 is impressed to address capacity 9b through address-line 7b. By impressing the address pulse 24 to address capacity 9b, the potential of the channel of magnification transistor 4b rises as compared with other Rhine, and a source follower circuit is constituted by a load transistor and magnification transistor 4b.
[0047] Therefore, an electrical potential difference with the signal charge of photodiode 5b almost equal to the signal level by which impedance conversion was carried out is outputted to a signal line 1. The signal outputted to this signal line 1 is outputted to a level signal line by being chosen with a level shift register through a noise rejection circuit.
[0048] By repeating successively actuation which was described above about each Rhine, the signal of all the photodiodes by which two-dimensional array was carried out can be read. Therefore, according to the solid state camera of the gestalt of this operation, detailed-ization of a unit cell can be attained by connecting the gate of the reset transistor of the unit cell which adjoins the gate and the direction lower part of a train of a readout transistor with common wiring.
[0049] Moreover, in case detailed-ization of a component is performed by making it such a configuration, the insulation resulting from the level difference within the short-circuit by spacing of wiring becoming narrow or a unit cell does not arise.
[0050] Furthermore, since the current which flows to a drain wire 2 by impressing a pulse to read-out / reset line is only a charge discharged through a reset transistor according to the solid state camera of the gestalt of this operation, a drain wire 2 does not apply a burden to a drain wire 2 that what is necessary is to perform only adjustment with the drain electrical potential difference of a reset transistor consequently.
The magnification mold solid state camera concerning <the gestalt of the 2nd operation>, next the gestalt of operation of the 2nd of this invention is explained.
[0051] Drawing 4 is drawing showing the configuration of the unit cell of the magnification mold solid state camera concerning the gestalt of operation of the 2nd of this invention. in addition, drawing 4 -- if it is, the configuration of 3 unit cells is shown and it is the magnification mold solid state camera of a 2-pixel 1 unit-cell configuration. Moreover, the same sign is attached and explained to the same part as drawing 1 .
[0052] In this drawing, although only three unit cells are shown, the unit cell of the magnification mold solid state camera of the gestalt of this operation shall be arranged in the shape of two-dimensional. As shown in this drawing, a unit cell 14 Read-out transistor 8a-1 for reading the charge accumulated in photodiode 5a-1 which changes light into a charge, 5a-2, photodiode 5a-1, and 5a-2 to detecting-element 13a, respectively, 8a-2, address capacity 9a that chooses Rhine which reads a signal charge, It has magnification transistor 4a which amplifies the detecting signal of a photodiode and is outputted to a signal line 1, and reset transistor 6a which resets the charge accumulated in detecting-element 13a.
[0053] Here, although the unit cell 14 was explained, the configuration with the same said of other unit cells shall be adopted. The gate of readout transistor 8a-1 is connected to readout line 11a. Readout line 11a transmits the signal for turning ON readout transistor 8a-1.
[0054] It connects with read-out / reset line 3a with the common gate of reset transistor 6b of the unit cell which adjoins in the gate and the direction of a train of readout transistor 8a-2. Read-out / reset line 3a transmits the signal from a perpendicular shift register. Read-out / reset line 3a transmits the signal from a perpendicular shift register.
[0055] Moreover, the end of address capacity 9a is connected to address-line 7a. Address-line 7a transmits the signal for choosing the readout line from a perpendicular shift register.
[0056] The gate of reset transistor 6a is connected to the readout transistor of the unit cell which adjoins the direction upper part of a train, and common wiring. This wiring transmits the signal for resetting the charge accumulated in detecting-element 13a from a perpendicular shift register.
[0057] Moreover, the drain of reset transistor 6a is connected to detecting-element 13a, and the source is connected to the drain wire 2 for discharging the charge accumulated in detecting-element 13a.
[0058] The gate of magnification transistor 4a is connected to detecting-element 13a, a drain is connected to a drain wire 2, and the source is connected to the signal line 1. The noise canceller for removing the noise of the signal outputted to the signal line 1 is formed in this signal line 1.
[0059] And the signal with which the noise outputted from the noise canceller was removed is outputted to a level signal line one by one through the level selection transistor driven by the selection pulse supplied from a level shift register.
[0060] Next, with reference to the timing chart of drawing 5 , actuation of the magnification mold solid state camera of the gestalt of this operation is explained. First, if the transfer pulse 31 is impressed in horizontal blanking interval H-BLK1 at read-out / reset line 3a, reset of the charge accumulated in detecting-element 13b will be performed, and the

charge accumulated in detecting-element 13b will be discharged by the drain wire 2.
[0061] Next, it reads through readout line 11b, a pulse 32 is read, and it is impressed by transistor 8b-1. By reading to readout transistor 8b-1 and impressing a pulse, the charge accumulated in photodiode 5b-1 is read to detecting-element 13b.
[0062] Next, the address pulse 33 is impressed to address capacity 9b through address-line 7b. By impressing the address pulse 32 to address capacity 9b, the potential of the channel of magnification transistor 4a rises as compared with other Rhine, and a source follower circuit is constituted by a load transistor and magnification transistor 4b.
[0063] Therefore, an electrical potential difference with the signal charge of photodiode 5b-1 almost equal to the signal level by which impedance conversion was carried out is outputted to a signal line 1. The signal outputted to this signal line 1 is outputted to a level signal line by being chosen with a level shift register through a noise rejection circuit.
[0064] Next, the transfer pulse 34 is impressed to read-out / reset line 3a, reset of the charge accumulated in detecting-element 13b is performed, and the charge accumulated in detecting-element 13b is discharged by the drain wire 2.
[0065] Next, it reads through a readout / reset line 3b, a pulse 35 is read, and it is impressed by transistor 8b-2. By reading to readout transistor 8b-2 and impressing a pulse, the charge accumulated in photodiode 5b-2 is read to detecting-element 13b.
[0066] Next, the address pulse 36 is impressed to address capacity 9b through address-line 7b. By impressing the address pulse 36 to address capacity 9b, the potential of the channel of magnification transistor 4a rises as compared with other Rhine, and a source follower circuit is constituted by a load transistor and magnification transistor 4b.
[0067] Therefore, an electrical potential difference with the signal charge of photodiode 5b-2 almost equal to the signal level by which impedance conversion was carried out is outputted to a signal line 1. The signal outputted to this signal line 1 is outputted to a level signal line by being chosen with a level shift register through a noise rejection circuit.
[0068] By repeating successively actuation which was described above about each Rhine, the signal of all the photodiodes by which two-dimensional array was carried out can be read. In addition, in explanation of the gestalt of above-mentioned operation, although the case where reset was performed to coincidence with a readout was explained, it is only resettable by being a certain timing and impressing a certain electrical potential difference to a readout / reset line by reading the threshold of a reset transistor and making it a value smaller than the threshold of a transistor.
[0069] Moreover, a readout and reset can be performed to coincidence by in such a case, reading to a readout / reset line and impressing an electrical potential difference higher than the threshold of a transistor performing both a readout and reset to coincidence. Such a drive is realizable by using the pulse of three values for the pulse impressed to a readout / reset line.
[0070] Therefore, according to the solid state camera of the gestalt of this operation, detailed-ization of a unit cell can be attained by connecting the gate of one reset transistor of the unit cell which adjoins the gate and the direction lower part of a train of a readout transistor with common wiring.
[0071] Moreover, in case detailed-ization of a component is performed by making it such a configuration, the insulation resulting from the level difference within the short-circuit by spacing of wiring becoming narrow or a unit cell does not arise.
[0072] Furthermore, since the current which flows to a drain wire 2 by impressing a pulse to read-out / reset line is only a charge discharged through a reset transistor according to the solid state camera of the gestalt of this operation, a drain wire 2 does not apply a burden to a drain wire 2 that what is necessary is to perform only adjustment with the drain electrical potential difference of a reset transistor consequently.
<Gestalt of the 3rd operation> drawing 6 is drawing showing the configuration of the unit cell of the magnification mold solid state camera concerning the gestalt of operation of the 3rd of this invention, and drawing 7 is drawing showing the layout of the unit cell of the magnification mold solid state camera in the gestalt of this operation.
[0073] in addition, drawing 6 -- if it is, the configuration of 2 unit cells is shown and it is the magnification mold solid state camera of a 1-pixel 1 unit-cell configuration. Moreover, the same sign is attached and explained to the same part as drawing 1 .
[0074] In this drawing, although only three unit cells are shown, the unit cell of the magnification mold solid state camera of the gestalt of this operation shall be arranged in the shape of two-dimensional. As shown in this drawing, this unit cell is equipped with photodiode 5a which changes light into a charge, address transistor 41a which chooses Rhine which reads a signal charge, magnification transistor 4a which amplifies the detecting signal of photodiode 5a and is outputted to a signal line 1, and reset transistor 6a which resets the charge accumulated in the detecting element.
[0075] The gate of address transistor 41a and the gate of reset transistor 6a are connected to the address / reset line 42a. The address / reset line 42a transmits the signal for turning ON address transistor 41a and reset transistor 6a.
[0076] That is, in the solid state camera of the gestalt of this operation, wiring of an address transistor and a reset

transistor is shared in one unit cell. Moreover, the above-mentioned address transistor and a reset transistor are transistors of an MOS mold, and the threshold of these transistors is made into a different value. About control of this threshold, the amount of doping in the channel of each MOS transistor is changed, or it controls by approaches, such as thickening thickness of an insulator layer.

[0077] Thus, an address transistor and a reset transistor are controllable independently by changing the threshold of an address transistor and a reset transistor.

[0078] That is, by impressing a reset pulse to the address / reset line 42a, reset transistor 41a is turned ON and the charge accumulated in the detecting element is discharged to a drain wire 2.

[0079] Next, address transistor 6a is turned ON by impressing an address pulse to the address / reset line 42a. Thereby, the charge corresponding to the charge accumulated in the detecting element is outputted to a signal line 1 from magnification transistor 4a.

[0080] By repeating successively actuation which was described above about each Rhine, the signal of all the photodiodes by which two-dimensional array was carried out can be read. In addition, although one unit cell was explained, the configuration with the same said of other unit cells shall be adopted here.

[0081] Therefore, according to the solid state camera of the gestalt of this operation, detailed-ization of a unit cell can be attained by connecting the gate of the address transistor in 1 unit cell, and the gate of a reset transistor with common wiring.

[0082] Moreover, in case detailed-ization of a component is performed by making it such a configuration, the insulation resulting from the level difference within the short-circuit by spacing of wiring becoming narrow or a unit cell does not arise.

[0083] Furthermore, according to the solid state camera of the gestalt of this operation, there are the following advantages compared with the case where wiring between the address means between two unit cells and a resetting means is shared.

[0084] That is, first, in the solid state camera in the gestalt of the 1st operation of a ****, and the gestalt of the 2nd operation, if a problem occurs in the function of common wiring by open circuit etc., the pixel defect which amounts to 2 pixels will occur, but according to the solid state camera of the gestalt of this operation, even if such a problem occurs, since it is that an image defect arises [1-pixel], a pixel defect can be suppressed to the minimum.

[0085] moreover, if wiring with a reset transistor and an address transistor is carried out to a share by 2 pixels, to the timing of the usual signal which resets after carrying out the address Since the address of the bottom is carried out and a top is reset, the direction of signal processing is made only in an one direction. And an up-and-down pixel cannot be read to coincidence to add and read the signal of 2 pixels or more of upper and lower sides. The application range of the device of having said that a pixel was extracted coarsely, or 2 pixels was compounded and processed according to an application for fast transfer is missing, consequently there is a problem of narrowing a user's application.

[0086] However, since according to the solid state camera of the gestalt of this operation wiring is shared within 1 unit cell and an up-and-down pixel can be read to coincidence, ** which adds and reads the signal of 2 pixels or more of upper and lower sides is made, and processing of having said that 2 pixels was compounded and processed for fast transfer can be realized.

[0087] Therefore, according to the solid state camera of the gestalt of this operation, the application range of a device can be extended, consequently the application of a user's solid state camera can be extended.

[0088] In addition, in explanation of the solid state camera of the gestalt of this operation, although the example which gave the address function to the MOS transistor was explained, as shown in drawing 8 , an address function may be given to capacity. In addition, also in drawing 8 , the same sign is given to the same part as drawing 6 .

[0089] Also in this case, the gate electrode of the reset MOS transistor in 1 pixel and the gate electrode of an address MOS transistor are connected by common address / reset line.

[0090] Even if it adopts such a configuration, the same effectiveness as the case where an address function is given to an address transistor can be acquired. Furthermore, the configuration of the unit cell of the solid state camera of the magnification mold at the time of transfer MOS transistor 51 being crowded for a unit cell is shown in drawing 9 . Also in this case, the same effectiveness as the case where an address function is given to an address transistor can be acquired by connecting the gate electrode of a reset MOS transistor, and the gate electrode of an address MOS transistor by common address / reset line.

[0091]

[Effect of the Invention] As a full account was given above, according to this invention, the solid state camera which made detailed-ization of a component realizable, and its drive approach can be offered. Moreover, according to this invention, the solid state camera which makes detailed-ization of a component realizable and does not apply a burden

to a drain wire, and its drive approach can be offered. Furthermore, according to this invention, few solid state camera and its drive approach of an image defect of a playback screen can be offered.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is drawing showing the configuration of the unit cell of the magnification mold solid state camera concerning the gestalt of operation of the 1st of this invention.
[Drawing 2] It is drawing showing the planar structure Fig. of the magnification mold solid state camera in the gestalt of this 1st operation.
[Drawing 3] It is the timing chart which shows actuation of the magnification mold solid state camera in the gestalt of this 1st operation.
[Drawing 4] It is drawing showing the configuration of the unit cell of the magnification mold solid state camera concerning the gestalt of operation of the 2nd of this invention.
[Drawing 5] It is the timing chart which shows actuation of the magnification mold solid state camera in the gestalt of this 2nd operation.
[Drawing 6] It is drawing showing the configuration of the unit cell of the magnification mold solid state camera concerning the gestalt of operation of the 3rd of this invention.
[Drawing 7] It is drawing showing the layout of the unit cell of the magnification mold solid state camera in the gestalt of this 3rd operation.
[Drawing 8] It is drawing showing the configuration of the unit cell at the time of giving an address function to the capacitor of the magnification mold solid state camera in the gestalt of this 3rd operation.
[Drawing 9] It is drawing showing the configuration of the unit cell in the case of having the transfer gate of the magnification mold solid state camera in the gestalt of this 3rd operation.
[Drawing 10] It is drawing showing the configuration of the unit cell of the conventional solid state camera.
[Drawing 11] It is drawing showing the layout of the unit cell of the conventional solid state camera.
[Description of Notations]
1 -- Signal line,
2 -- Drain wire
3a-3c -- Read-out / reset line,
4a-4c -- Magnification transistor,
5a-5c -- Photodiode,
5a-1, 5a-2 -- Photodiode,
5b-1, 5b-2 -- Photodiode,
5c-1, 5c-2 -- Photodiode,
6a-6c -- Reset transistor,
7a-7c -- Address line
8a-8c -- Read-out transistor,
8a-1, 8a-2 -- Read-out transistor,
8b-1, 8b-2 -- Read-out transistor,
8c-1, 8c-2 -- Read-out transistor,
9a-9c -- Address capacity,
10 -- Component isolation region,
11a-11c -- Read-out line,
12 -- Unit cell
13a-13c -- Detecting element,
14 -- Unit cell

21 -- Transfer pulse,
22 -- Address pulse,
23 -- Transfer pulse,
24 -- Address pulse,
31 -- Transfer pulse,
32 -- Readout pulse,
33 -- Address pulse,
34 -- Transfer pulse,
35 -- Readout pulse,
36 -- Address pulse,
41a -- Address transistor,
111 -- Signal line,
112 -- Drain wire
113a-113c -- The address / reset line,
114a-114c -- Magnification transistor,
115a-115c -- Photodiode,
116a-116c -- Reset transistor,
117a-117c -- Address transistor.

[Translation done.]

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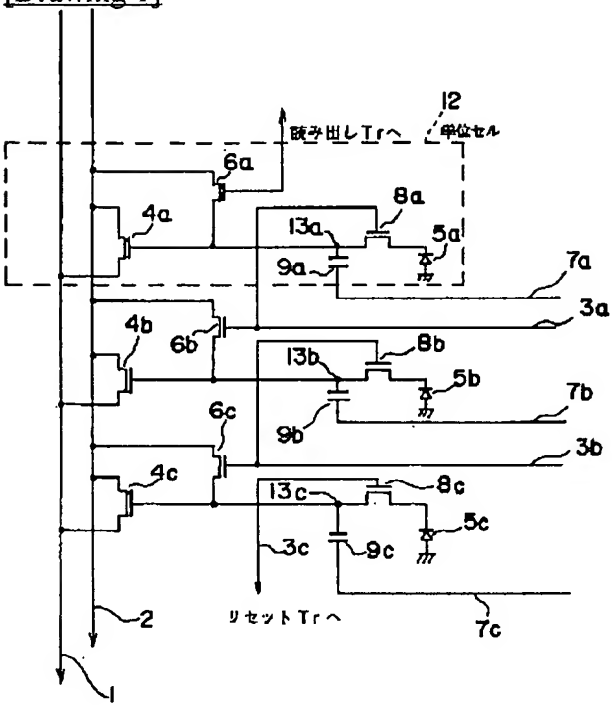
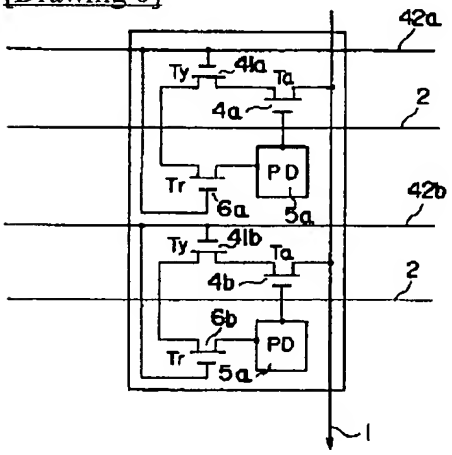
DRAWINGS

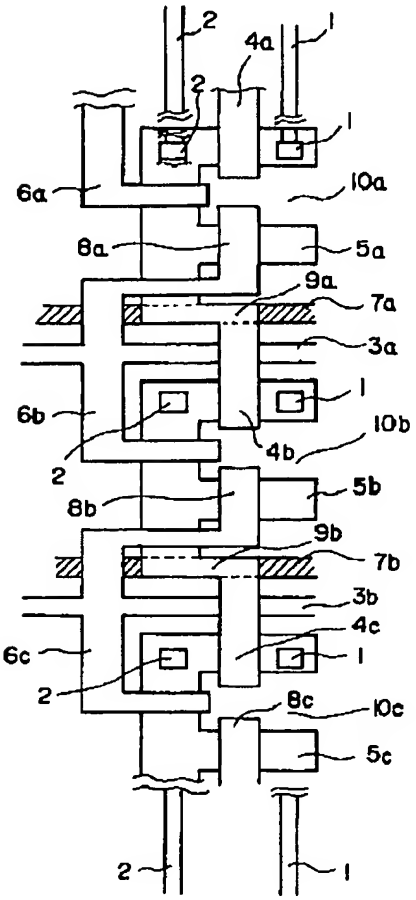
[Drawing 1]



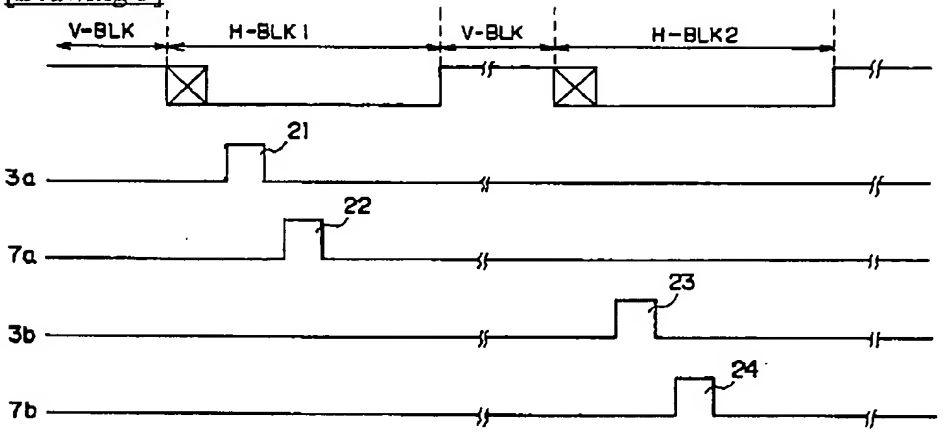
[Drawing 6]



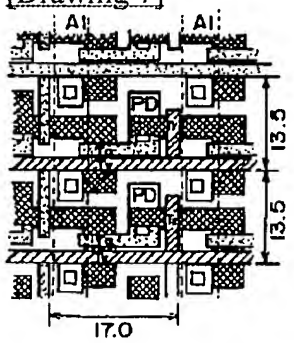
[Drawing 2]



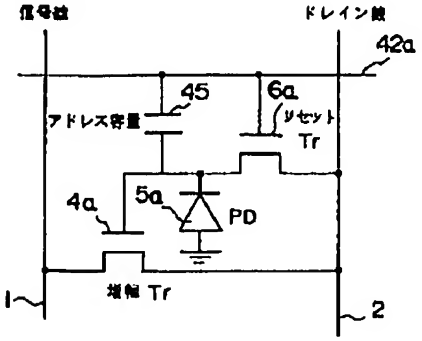
[Drawing 3]



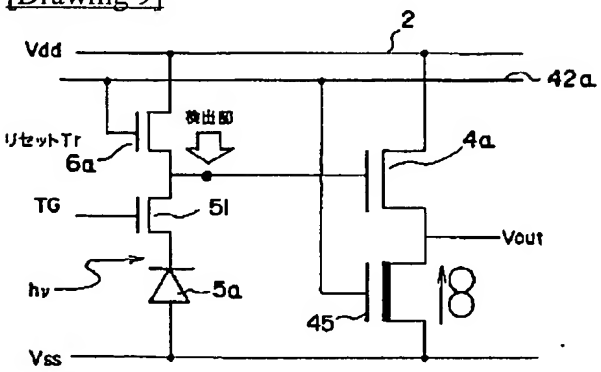
[Drawing 7]



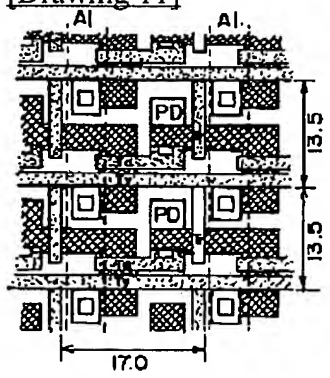
[Drawing 8]



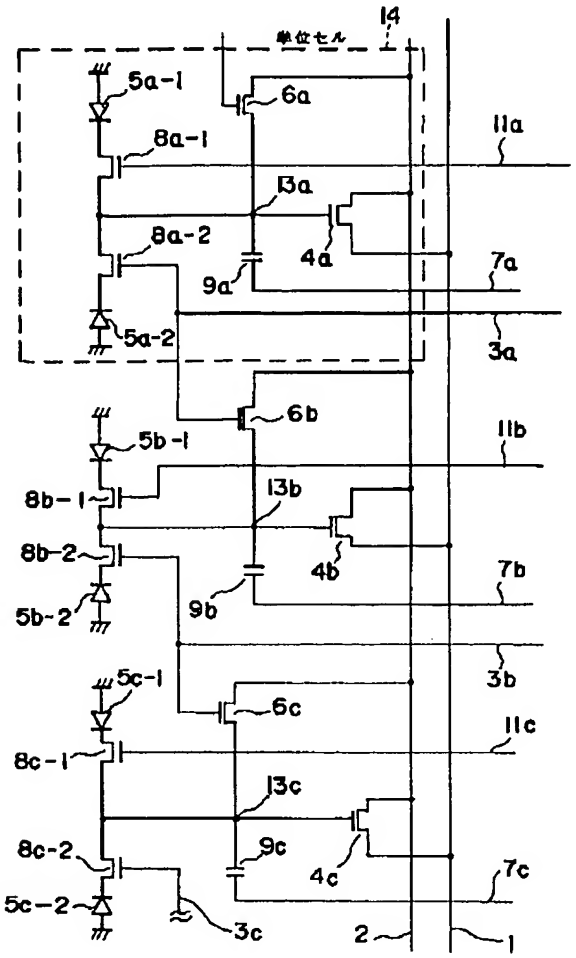
[Drawing 9]



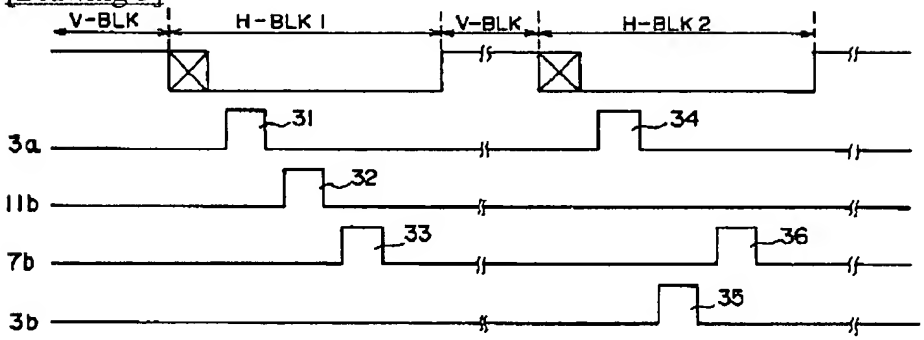
[Drawing 11]



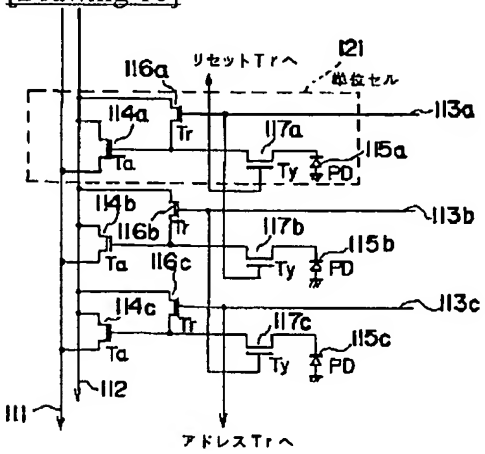
[Drawing 4]



[Drawing 5]



[Drawing 10]



[Translation done.]